

## MOTT SiGe SIMMWICs

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### ABSTRACT

Mixer diodes in SIMMWIC (silicon millimeter wave integrated circuit) technology with barrier height reducing  $n^+$  cap layers and SiGe top layers are investigated. The standard Mott diode with Ti-metallization has a barrier height of 0.5 V. By introducing an  $n^+$  cap layer of 10 nm thickness and a doping concentration of  $2 \cdot 10^{18} \text{ cm}^{-3}$  a barrier height reduction of 0.08 V is achieved, while a 8 nm thick SiGe layer with 30 % Ge increases the barrier height about 0.06 V. Conversion loss of 6.5 dB is measured in single ended mixers with an LO power of 10 dBm. The 1/f noise corner frequency is at 3 kHz for diode currents of 1 mA.

### INTRODUCTION

The integration of avalanche transit time diodes on high resistivity silicon substrate has been demonstrated previously [1]. Subharmonic injection locking of free running oscillator chips with SiGe HBT oscillator MMICs potentially can improve the frequency stability, spectral purity and temperature behavior [2]. For the receiver part of the front-ends, mixer diodes are developed. In FMCW radars 1/f noise is limiting the range of the anticipated intelligent cruise control systems. In this work we describe the influence of barrier lowering delta-doped

layers, SiGe layers and passivation techniques on the RF (76 GHz) and noise performance of integrated silicon Schottky diodes of the Mott type (fully depleted epitaxial layer at zero bias).

### DEVICE DESIGN

The investigated Schottky barrier diodes are designed and fabricated for mixer applications at 76 GHz. The diodes should operate without DC bias (zero bias operation). Therefore to achieve moderate LO power a low barrier height is necessary. But also the noise performance of the diode is of great importance, since in FMCW radars 1/f noise is limiting the range. The diodes are fabricated on high resistivity silicon using the layer sequence shown in Fig. 1.

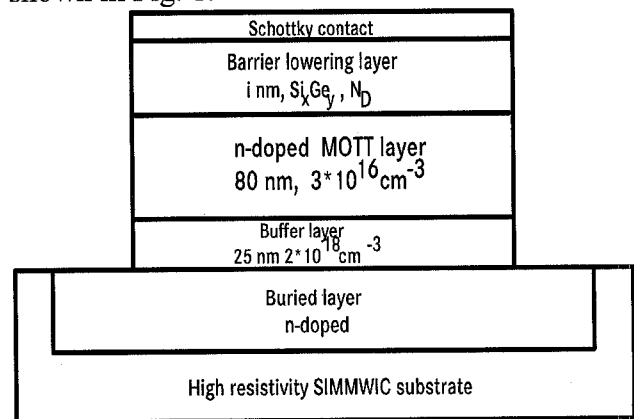


Fig. 1: Layer sequence of the investigated Schottky barrier diodes

## FABRICATION PROCESS

The buried layer is formed by As-implantation and a subsequent diffusion process. The resulting sheet resistance is  $4.3 \Omega/\square$  and a maximum As concentration at the surface of  $1 \times 10^{20} \text{ cm}^{-3}$  is achieved. The low sheet resistance and high surface concentration lowers series resistance and contact resistance of the diode. The whole layer sequence of the Schottky barrier diode is grown by silicon molecular beam epitaxy (Si-MBE). MBE offers low growth temperature, interface abruptness and precise control of doping profile and thickness with nm resolution. On a 25 nm thick,  $2 \times 10^{18} \text{ cm}^{-3}$  doped  $n^+$  buffer layer, a 80 nm thick, lightly doped semiconductor n-layer is grown. The growth temperature was  $550^\circ\text{C}$ . For the design of the mm-wave Schottky barrier diodes the effect of the voltage dependent depletion layer is taken into account. A complete depletion of the thin epitaxial layer (Mott diode) is expected for doping levels up to  $7 \times 10^{16} \text{ cm}^{-3}$  (zero bias, 0.5 V Schottky barrier height). Schottky barrier lowering is investigated by an additional surface doping spike. (10 nm,  $2 \times 10^{18} \text{ Sb/cm}^3$  up to  $2 \times 10^{19} \text{ Sb/cm}^3$ ). Also the influence of undoped SiGe cap layers on the Schottky barrier height were investigated.

The Schottky anode contact is formed by photolithographic patterning and a lift-off process with 50 nm Ti, 50 nm Pt and 200 nm Au. Then the epitaxial layer is plasma etched using the Schottky contact as an etch mask. The epitaxial layer is removed all over the wafer except underneath the Schottky contact. Thus access to the  $n^+$  buried layer (ohmic contact) is achieved. The ohmic contact is formed using a second lift-off process with Ti, Pt, and Au metallization (Fig. 2). Lateral isolation which is important for monolithic diode pairs is obtained by an implanted guard ring. The diodes are then

passivated with a low temperature PECVD silicon nitride. Flip chip diodes are realized with gold metallization layers.

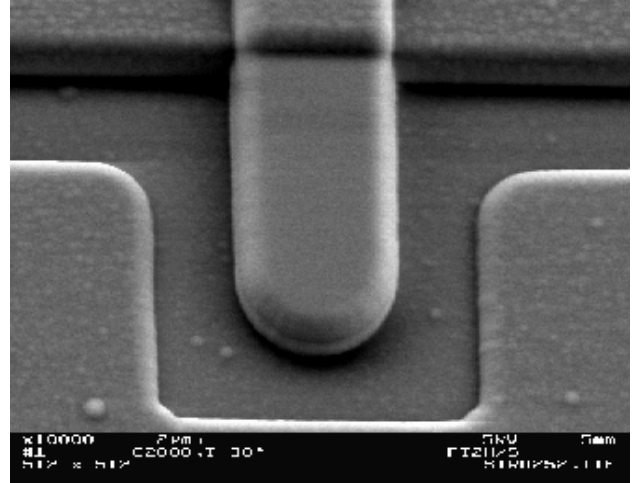


Fig. 2: SEM of the passivated Schottky anode finger surrounded by the ohmic contact metallization

## DIODE CHARACTERIZATION

DC characteristics of the diodes are evaluated from I-V and C-V measurements. Series resistance  $R_s$ , barrier height  $\Phi$ , ideality factor  $n$  and junction capacitance  $C_j$  strongly depend on doping parameters, diode geometry and anode metallization. For n-diodes with Titanium as Schottky anode metal a barrier height of 0.5 V is determined from the saturation current which corresponds to the theoretical value [3]. Tab. 1 lists the measured values for diodes with different cap layers.

In all diodes titanium is used as Schottky contact metallization. The barrier height reduction of 0.08V with the  $n^+$  cap layer corresponds to published values [4]. The barrier lowering is significant because it reduces the forward voltage of the devices so that it is possible to operate the diodes as mixers without

Tab. 1: Barrier heights of Mott diodes with different cap layers

Epitaxial Layer	Cap Layer	Barrier height
80 nm, $3 \cdot 10^{16} \text{ cm}^{-3}$	-	0,5 V
80 nm, $3 \cdot 10^{16} \text{ cm}^{-3}$	10 nm, $2 \cdot 10^{18} \text{ cm}^{-3}$	0,42 V
80 nm, $3 \cdot 10^{16} \text{ cm}^{-3}$	10 nm, $2 \cdot 10^{19} \text{ cm}^{-3}$	ohmic cont.
80 nm, $3 \cdot 10^{16} \text{ cm}^{-3}$	8 nm i-SiGe(30%)	0,56 V

bias at a reasonable level of local oscillator power even at elevated temperatures. With the SiGe cap layer (30% Ge) an increase of barrier height by 0.06 V is observed. In [5] Schottky diode characteristics of Ti on p-strained SiGe layers are reported. With 18 % Ge a barrier height reduction from 0,62 to 0,60 V at room temperature is reported. This is in agreement with the observed barrier height increase for Ti on n-type SiGe layers.

The diodes have also been characterized by S-parameter measurements up to 50 GHz. Fig 4 shows typical values for the equivalent circuit elements as a function of forward voltage using the equivalent circuit diode model of Fig 3.

### NOISE PERFORMANCE

Mott SiGe SIMMWICs show an extremely good low frequency noise behavior: the noise floor close to the carrier is about 8-10 dB below the values of comparable III-V diodes. Fig. 5 shows typical  $1/f$ -noise measurements of a diode for different diode currents. Fig 6 shows the  $1/f$  noise behavior of different diodes at a diode current of 1 mA. The  $1/f$  noise corner frequency is 3 kHz.

Diodes with a Schottky anode area of  $12 \mu\text{m}^2$  were tested at 94 GHz in a single ended mixer:

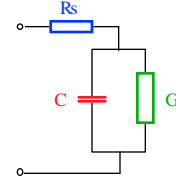


Fig. 3: Equivalent circuit model of Schottky diode

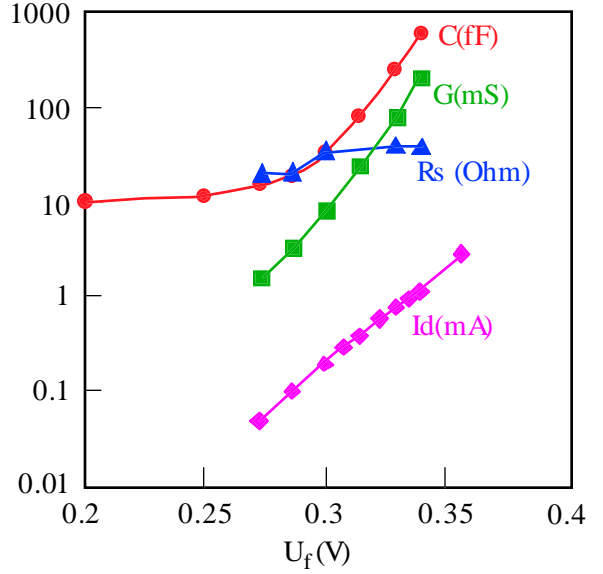


Fig.4: Typical values of the equivalent diode model in forward operation

With an LO power of 1 mW a conversion loss of 10 dB (SSB) is measured, with an LO power of 10 mW a conversion loss of 6.5 dB is found. No bias was applied to the diodes (zero bias operation). The noise performance of barrier height reduced diodes is 3 - 5 dB worse than those without barrier height reduction (Fig. 7).

### CONCLUSION

The introduction of SiGe layers on top of n-Schottky layers causes an increase of the barrier height. The achieved barrier height reduction by an n-doped spike (silicon) leads to an increase of the close to carrier noise. In conclusion, the Mott diode without any cap layer is best suited for the  $1/f$  noise limited system applications.

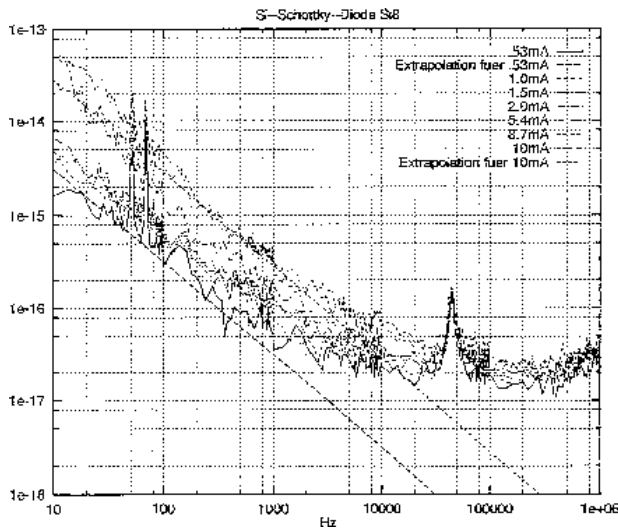


Fig. 5 :  $1/f$  noise behavior of SIMMWIC Schottky barrier diodes for different diode currents

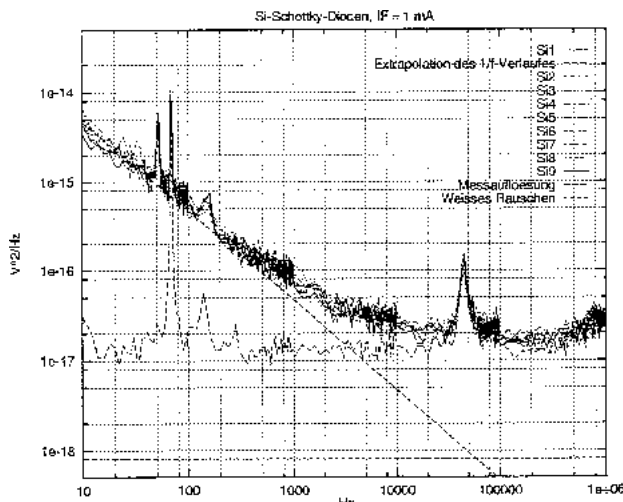


Fig. 6 :  $1/f$  noise behavior of different SIMMWIC Schottky barrier diodes for a diode current of 1 mA. The  $1/f$  noise corner frequency is 3 kHz

### ACKNOWLEDGEMENT

Thanks to S. Lindenmaier, D. Eisbrenner and R. Schödlbauer for technical assistance, H. Schumacher and U. Erben from University of Ulm for performing the noise measurements, R.

Jester and H. Matti from DASA Ulm for the mixer data and P. Heyman, H. Prinzler and R. Doerner for S-parameter characterization of the Schottky diodes.

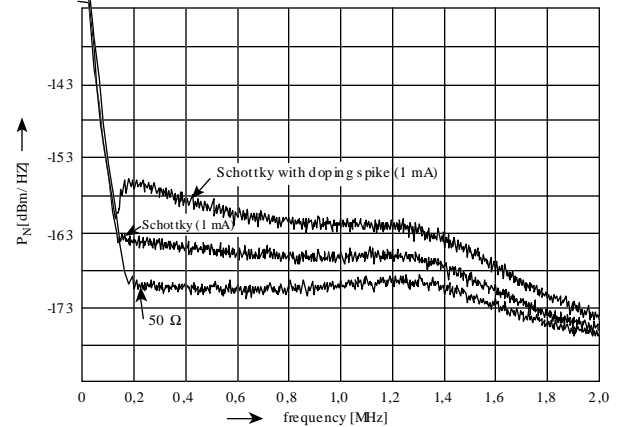


Fig. 7: Noise power of SIMMWIC Schottky diodes with and without doping spike compared to a 50  $\Omega$  system at 1 mA respectively

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